What is claimed is:

[Claim 1] 1. A method for accessing memory cells within a dynamic hardware memory block operated with a precharge mechanism, in which differential read and write access operations are performed by activating a true bitline and a complement bitline, the method comprising:

determining whether a next memory access operation occurring subsequent to a current access operation is a read access operation or a write access operation; and
performing a precharge of the true and complement bitlines only when a read access operation follows the current access operation.

[Claim 2] 2. The method according to claim 1, wherein a static random access memory (SRAM) array comprises the memory cells.

[Claim 3] 3. The method according to claim 1, in which a first precharge control signal is combined with a 'read cycle (n+1) control signal to evaluate whether a next memory access cycle comprises a read access or a write access.

[Claim 4] 4. The method according to claim 3, wherein the first precharge control signal and the read cycle n+1 control signal are combined to yield a second precharge signal.

[Claim 5] 5. The method according to claim 3, wherein the read cycle (n+1) control signal is asserted according to an operating mode of the memory array, such that a write access operation occurring over a plurality of system clock cycles results in a continuous assertion of the next read cycle (n+1) control signal until the write access operation is complete.

[Claim 6] 6. The method according to claim 3, wherein the read cycle (n+1) control signal is asserted two system clock cycles in advance of a next

memory access operation during a delay between when an address of the memory array is specified and a current access operation is complete.

[Claim 7] 7. The method according to claim 3, wherein the next read cycle (n+1) control signal is asserted

after a delay of one clock cycle during a period of time when no memory operation is performed.

[Claim 8] 8. An integrated circuit memory array adapted for low power operation, comprising:

a plurality of addressable memory cells arranged in rows and columns, the memory cells segmented into a plurality of memory blocks;

a plurality of column lines, each coupled to a corresponding column of memory cells;

a plurality of row lines, each coupled to a corresponding row of memory cells;

a precharge circuit coupled to the plurality of row lines, the precharge circuit provided to assert the plurality of row lines in a memory block to a high logic level following a memory access operation;

a first precharge signal controller coupled to the precharge circuit, the first precharge signal controller provided to generate a first precharge control signal;

a read cycle signal controller for generating a read cycle (n+1) signal when a next memory access operation is read access operation; and

a logic element to evaluate the first precharge control signal and the read cycle control (n+1) signal, the logic element asserting a second precharge

control signal when a next memory access is a read access operation for controlling the precharge circuit.

[Claim 9] 9. The memory array according to claim 8, wherein the logic element comprises an AND gate.

[Claim 10] 10. The memory array according to claim 8, wherein the logic element comprises a multiplexer.

[Claim 11] 11. The memory array according to claim 8, wherein the memory array is a static random access memory (SRAM).